An All-Digital Unified Clock Frequency and Switched-Capacitor Voltage Regulator for Variation Tolerance in a Sub-Threshold ARM Cortex M0 Processor

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Abstract

An all-digital switched-capacitor (SC) based clock frequency (F_{clk}) and supply voltage (V_{dd}) regulator unifies F_{clk} and V_{dd} generation into a single control loop to reduce the V_{dd} margin for variations in a sub-threshold ARM Cortex M0 processor. The fully-integrated unified clock and power (UniCaP) architecture allows continuous V_{dd} scalability without a low-dropout (LDO) regulator. Measurements from a 65nm test chip demonstrate a 16% V_{dd} reduction (94% V_{dd} margin recovery) and a 3.2× increase in F_{clk} operating range.

Introduction

Conventional F_{clk} and V_{dd} regulation consists of two separate and independent control loops. As a result, the F_{clk} control loop is unaware of the impact of V_{dd} or temperature (T) changes on path timing margin. Thus, conventional designs require a V_{dd} margin to ensure correct operation at a target F_{clk}, motivating adaptive techniques to reduce this margin [1, 2]. Recent work combines the F_{clk} and V_{dd} regulation into a single control loop based on an LDO [3] and a buck converter [4]. By generating the core clock with a V_{dd}-powered tunable-replica oscillator (TRO), F_{clk} intrinsically adapts to V_{dd} and T variations to compensate for critical-path-delay changes to maintain a nearly constant timing margin independent of the V_{dd} regulation bandwidth. These systems continuously adjust V_{dd} to lock F_{clk} to a target reference frequency (F_{REF}). In contrast to LDO or buck regulators, SC converters offer high efficiency and low-cost on-die integration. Traditional SC designs, however, suffer from poor load regulation and support a limited set of discrete voltages, which negatively affects dynamic voltage and frequency scaling (DVFS) opportunities. Configurable SC techniques [5], use of LDOs [6], or controlling SC output impedance in traditional two-loop systems overcome discrete SC ratio limitations, but these options limit the load-regulation range and are either complex, result in excessive headroom, or require large V_{dd} droop margin. This paper presents the first all-digital, SC-based UniCaP architecture (UniCaP-SC) to enable continuous V_{dd} scalability and V_{dd} margin reduction for high-efficient and low-cost IoT processors.

Architecture and Implementation

UniCaP-SC (Fig. 1) relies on a V_{dd}-powered TRO to provide an elastic F_{clk} for robust load and line regulation. Since V_{dd} and T variations modulate the clock period ($T_{clk}=1/F_{clk}$) and the critical-path delays similarly, timing margin remains nearly constant. The SC frequency (F_{SC}) controls the resistive voltage drop across the SC output impedance to provide continuous linear V_{dd} regulation in the 0.56V-0.44V range without an LDO and associated headroom requirements. V_{dd}-adaptive clocking readily addresses worsening V_{dd} droop from increased SC output impedance. Instead of regulating V_{dd} to a reference voltage, UniCaP-SC employs a frequency-locked loop (FLL) to control V_{dd} to lock F_{clk} to F_{REF}.

Tracking a noisy V_{dd} requires a time-to-digital converter (TDC) with a wide capture range. The implemented coarse-grained cycle-counting TDC (Fig. 2) detects phase errors up to eight reference clock cycles. The computationally-derived frequency is accumulated into a resulting phase error ($\Delta\phi_n$) for proportional control. A digital delta-sigma modulator (DSM) drives a 7-bit digitally controlled oscillator (DCO) to provide 16-bits of F_{SC} control resolution.

The design uses a standard 8-way interleaved 2:1 converter using NMOS capacitors (Fig. 3). Split-level SC gate drive reduces switching loss by using a mid-level rail (V_{mid}, ideally equal to $V_{in}/2$) to buffer the SC clocks ϕ_{12} and ϕ_{01} in the V_{mid}-to-V_{in} and 0-to-V_{mid} ranges, respectively. An externally dedicated V_{mid} voltage [7] is not cost effective and powering the SC clocks with the internal SC rail (i.e., V_{dd}) introduces efficiency-degrading inter-level skew that causes capacitor shorting from overlapped clocks (Fig. 4). The proposed floating V_{mid} (Fig. 5) allows charge-recycling between upper and lower buffers across all phases to produce a stable $V_{in}/2$ independent of V_{dd}. Measured oscilloscope traces demonstrate V_{mid} rapidly settling to $V_{in}/2$ after power-up (Fig. 6).

Measured Results

In the 65nm test chip (Fig. 11), the UniCaP-SC generates the F_{clk} and V_{dd} to operate an ARM Cortex M0 processor and an FFT accelerator in sub-threshold. Since intrinsic F_{clk} modulation avoids timing-margin degradation during large V_{dd} droops, no explicit decoupling capacitance is added. A programmable load-current (I_L) module injects V_{dd} droops based on either a constant I_L step or an I_L step equal to the processor active current to capture the I_L dependency on V_{dd} and F_{clk} scaling. Measured SC efficiency (η_{SC}) (Fig. 7) demonstrates that the proposed floating V_{mid} design enables ~10% η_{SC} gains across I_L at V_{dd} = 0.525V, as compared to a split rail with V_{dd} connected to V_{mid}. Across V_{dd}, η_{SC} benefits are more pronounced, ranging from ~10% to ~30% between 0.56V and 0.44V. In comparison with a conventional two-loop approach (independent F_{clk}, V_{dd} regulation), measurements demonstrate that UniCaP-SC provides a 40mV V_{dd} reduction from -15°C to 45°C while remaining locked at F_{clk} = 15MHz (Fig. 8). Maximum F_{clk} (F_{max}) versus V_{dd} measurements were made (Fig. 9) with a V_{dd} droop resulting from an I_L step equal to the processor active current and T variation from -15°C to 45°C. UniCaP-SC reduces V_{dd} by 87mV (16%) at F_{max} = 8.2MHz, recovering 94% of the V_{dd} margin in the conventional design. In addition, UniCaP-SC extends the F_{max} range by 3.2×. The measured improvement in system energy per cycle (Fig. 10), capturing both η_{SC} and processor energy (E_{proc}), is 12.3% from mitigating V_{dd} droops alone at F_{max} = 8.2MHz. Measured oscilloscope traces (Fig. 12) demonstrate on-the-fly DVFS functionality and transient response to a 1mA I_L step. A comparison with related work (Fig. 13) highlights competitive efficiencies while providing tolerance to V_{dd} and T variations.

References

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Acknowledgments

Arijit Raychowdhury and Carlos Tokunaga for helpful discussions. Funded by SRC (task 2712.006) and by Qualcomm Technologies, Inc.

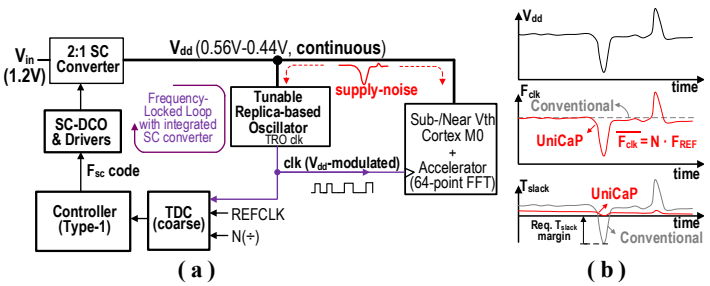

Fig. 1: (a) UniCaP-SC architecture with (b) an elastic clock to maintain a nearly constant timing margin across V_{dd} or T variation

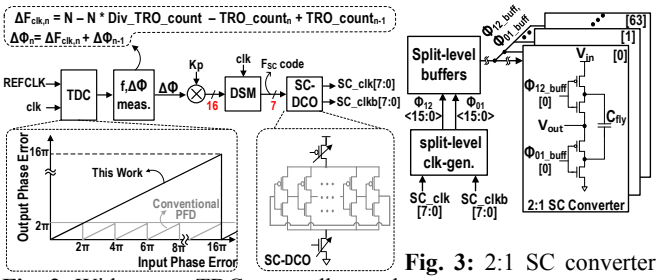

Fig. 2: Wide-range TDC, controller, and with split-rail clocks DCO for SC switching frequency control

Fig. 3: 2:1 SC converter

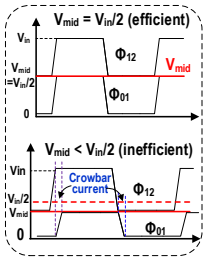

Fig. 4. Inter-level clock skew degrades SC efficiency when $V_{mid} < V_{dd}/2$

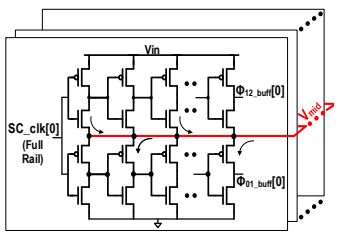

Fig. 5: Proposed split-rail charge-recycling with floating V_{mid} connection across all phases

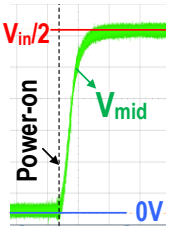

Fig. 6: Measured oscilloscope trace of floating V_{mid} scheme

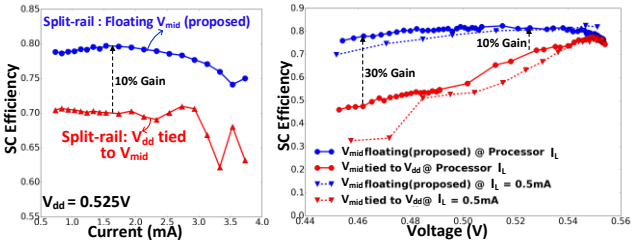

Fig. 7: Measured SC-converter efficiency vs. (a) I_L and (b) V_{dd} for two split-rail designs: (i) proposed with V_{mid} floating and (ii) V_{mid} connected to V_{dd}

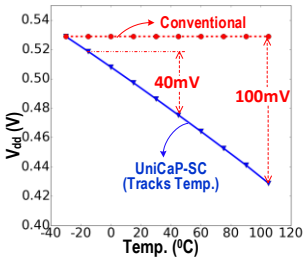

Fig. 8: Measured V_{dd} vs. Temp. for a target F_{clk} of 15MHz across the entire T range

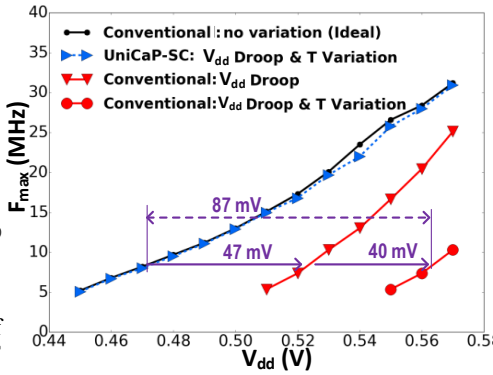

Fig. 9: Measured maximum F_{clk} (F_{max}) vs. V_{dd}

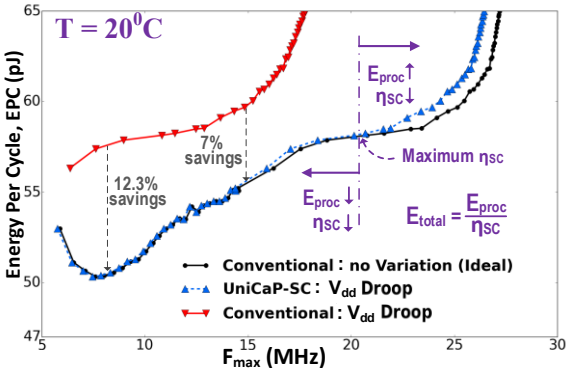

Fig. 10: Measured Energy per Cycle of the system

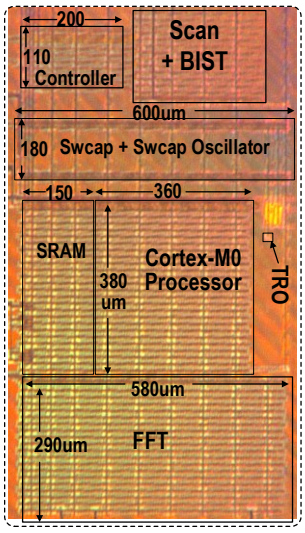

Fig. 11: Test-chip die photo.

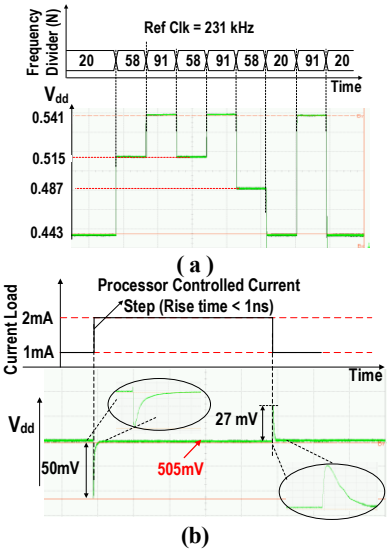

Fig. 12: Measured oscilloscope traces demonstrating (a) on-the-fly DVFS by varying N and (b) transient V_{dd} response to a 1mA I_L step.

	VLSI Symp '17 [8]	VLSI symp '15 [9]	JSSC'14[7]	This work
Process Technology	65nm CMOS	28nm FDSOI	22nm Trigate CMOS	65nm CMOS LP
Input Voltage (V)	1.2	1, 1.8	1.23	1.2
Output Voltage (V)	0.55,0.35, 0.25	0.45-1	0.45-1	0.44-0.56 (Continuous)
SC converter operation	Near Threshold, Sub-Threshold	Super-threshold	Super-threshold	Near Threshold, Sub-threshold
All-Digital	No	No	Yes	Yes
Process and T tracking	No	No	N/A	Yes
V_{dd} Margin reduction (for 100% I_L) *	N/R	N/R	N/A	98.9% (peak) 94.76% (mean) 89% (worst)
T Margin Reduction *	No	No	N/A	100mV (-20C to 110C)
REFCLK Freq. Tracking	No	No	N/A	Yes
Efficiency	Peak 82% (0.55V)	Peak 90%	Peak 70% (0.55V)	Peak 82.4% (0.5V,1.1mA)

*Margin Reduction = $\frac{V_{dd,ideal} - V_{dd,UniCaP}}{V_{dd,ideal} - V_{dd,conventional}} \times 100\%$

Fig. 13: Comparison with related works