21.5 A 1.1GHz Charge-Recovery Logic

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Boost Logic is a charge-recovery circuit family capable of operating at GHz-class frequencies [1]. In this paper, the design and experimental validation of a 1.1GHz Boost Logic test chip is reported. The test chip is fabricated in a 0.13µm CMOS process with an integrated inductor and an on-chip clock generator. This chip is an implementation of a dynamic charge-recovery logic family operating successfully in the GHz regime. Previous charge-recovery circuit implementations with on-chip clock generators have been reported to operate at frequencies no greater than 130MHz [2, 3, 4]. In addition to fast operation, Boost Logic achieves high energy efficiency due to its (i) balanced clock load, (ii) decoupled logic evaluation and charge-recovery stages, and (ii) absence of diodes. This Boost Logic chip recovers 60% of the energy supplied to it at each clock cycle.

Figure 21.5.1 shows a Boost Logic gate. It consists of a dual-rail logic stage that operates in tandem with a charge-recovering boost stage. The logic stage performs functional evaluation and is powered by a dc supply $V_C = V_{dd}' - V_{ss}' = V_{th}$, centered at $V_{dd}/2$. The Boost stage then amplifies the potential difference between *out* and $\overline{out}$ to V_{dd}. Figure 21.5.2 illustrates the operation of a Boost inverter. During the boost stage, the header and footer transistors of the logic stage are off, isolating the outputs from the logic rails. As $\phi(\overline{\phi})$ transitions to V_{ss} (V_{dd}), transistor M3 (M1) discharges (charges) the output node $\overline{out}$ (*out*). The output nodes track the power-clocks until their potential difference reaches V_{th}, at which time all transistors in the boost stage are in cut-off and remain so during the subsequent logic stage. As ϕ falls below V_{ss}', logic evaluation begins, resolving the output nodes to a potential difference of nearly V_{th}, and as ϕ crosses V_{dd} ', the boost stage drives the output nodes to the full rail. By relying on resonance to drive the output nodes to a voltage difference V_{dd}, the boost stage efficiently provides a high gate overdrive to fanout logic stages. Although $V_C = V_{th}$, all transistors conduct in the super-threshold linear region due to this high gate overdrive.

Fabricated in a 0.13µm 8M (copper, 2 thick) 1.2V CMOS process, this test chip consists of 8 gate chains with a total of 1680 Boost gates comprising AND, OR, XOR and INV. The logic gates and clock generator occupy a total area of 315×320µm². Complementary resonant clocks ϕ and $\overline{\phi}$ are generated with an H-bridge topology. Pulses *a* and *b* at 180° are derived from a reference clock and drive the clock generator switches in tandem, periodically replenishing dissipated energy in the system. The frequency *f* of the reference clock is programmable in the range 700MHz ≤ *f* ≤ 1.3GHz.

The resonant clocks oscillate at the reference frequency *f*. For efficient operation, *f* should be near the natural frequency $f_0 \approx 1/2\pi\sqrt{LC}$ where C is the total capacitance resonated with inductance L. To explore the impact of design trade-offs on energy efficiency, the clock generator is designed with programmable switch widths (0µm<*W*<400µm) and pulse duty cycle (0%<*D*<50%). The GHz frequency target necessitates the deployment of an integrated inductor in charge-recovery logic design. A 2.4nH 2.5-turn inductor is included in two top-level metal layers to resonate 29pF (per-phase) of clock capacitance.

Figure 21.5.4 shows measured supply current and corresponding energy dissipation versus operating frequency for the test chip. Reported energy-dissipation numbers include the energy dissipated in the resonant network, clock generator, and clock generator switches. Each point in the plot corresponds to the minimum supply current or the energy dissipation of the circuit over all possible V_{dd}, V_C, *D,* and *W* values that result in correct operation, as verified by observing the required signature waveform. The minimum current is measured at 800MHz. The corresponding energy dissipation, is expectedly higher at about 850MHz. The load can be nevertheless driven at frequencies above at the expense of additional energy dissipation. By scaling the supply voltage to 1.5V, correct operation at 1.3GHz is verified. When resonating at 850MHz, the circuit recovers 60% of the peak energy stored in the system, which translates to a Q factor of approximately 3.93. By forcing the circuit to operate at 1GHz, the recovery drops to 40%.

Figure 21.5.5 shows the measured energy dissipation as a function of V_C and V_{dd}. The optimal V_C results from the tradeoff between improved recovery efficiency at high V_C and lower conventional energy dissipation at lower V_C. The optimal V_{dd} arises from the tradeoff between reduced I^2R losses due to lower oscillation amplitude at low V_{dd} and higher gate overdrive at high V_{dd}, which enables efficient charge recovery in fanout gates. At 850MHz, the minimum measured energy dissipation is observed for V_c = 0.45V, V_{dd} =1.4V, *D* = 22%, and *W* = 225µm .

The I^2R dissipation losses in the clock network are replenished by periodically injecting current into the inductor. The amount of energy replenished in each cycle is a function of the replenishing switch width *W* and the duty cycle of the pulse duty cycle *D*, shown in Fig. 21.5.3. Figure 21.5.6 shows the shmoo plot obtained by varying the two parameters while ensuring correct operation at 850MHz. Each point in the plot signifies correct operation for the corresponding pair (*W*, *D*). All points denoted by the same symbol fall within a 4pJ-wide band of measured energy dissipation. The iso-energy bands illustrate the tradeoff between *W* and *D*. From this scatter plot it can be inferred that both *W* and *D* play a significant role in controlling clock generator dissipation.

Figure 21.5.7 shows a micrograph of the 1.1GHz charge-recovery chip. Including the moat around it, the 2.4nH on-chip inductor occupies about 0.078mm². Inductor size decreases for higher operating frequencies or larger designs. The complementary clock phases, ϕ and $\overline{\phi}$, are routed from opposite sides of the inductor with a main trunk for each phase running along the length of the chains. Alternating shielded spines of ϕ and $\overline{\phi}$ are striped across the active logic area with a 16µm pitch.

The implementation of a fully integrated GHz-class charge-recovery dynamic logic is presented. Voltage and current measurements indicate that at the natural frequency of the design, 60% energy recovery is achieved. Correct operation is verified up to 1.3GHz.

Acknowledgments:
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References:
[1] V. S. Sathe, et al., "A GHz-Class Charge Recovery Logic," *ISLPED*, pp. 91-94, Aug., 2005.
[2] S. Kim, et al., "True Single-Phase Adiabatic Circuitry," *Transactions on VLSI Systems*, pp. 52-63, Feb., 2001.
[3] D. Suvakovic, C. Salama, "Two Phase Non-Overlapping Clock Adiabatic Differential Cascode Voltage Switch Logic (ADCVSL)," *ISSCC Dig. Tech. Papers,* pp. 364-365, Feb., 2000.
[4] D. Maksimovic, V. Oklobdzija, B. Nikolic, and K. Current, "Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply," *Transactions on VLSI Systems*, Aug., 2000.

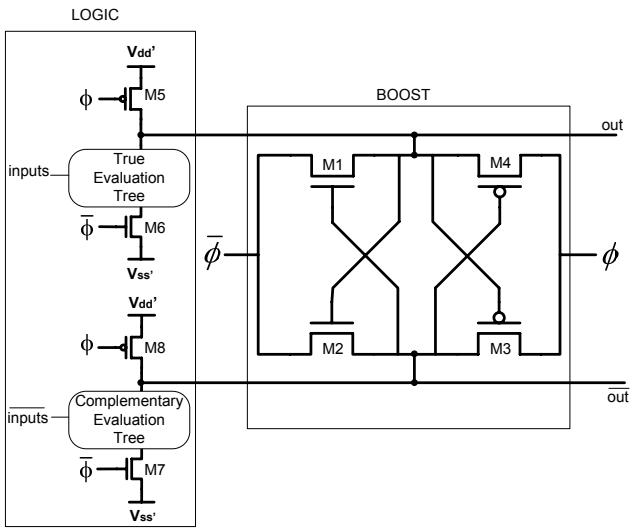


Figure 21.5.1: Schematic diagram of a Boost-Logic gate with NMOS-only pulldown evaluation trees.

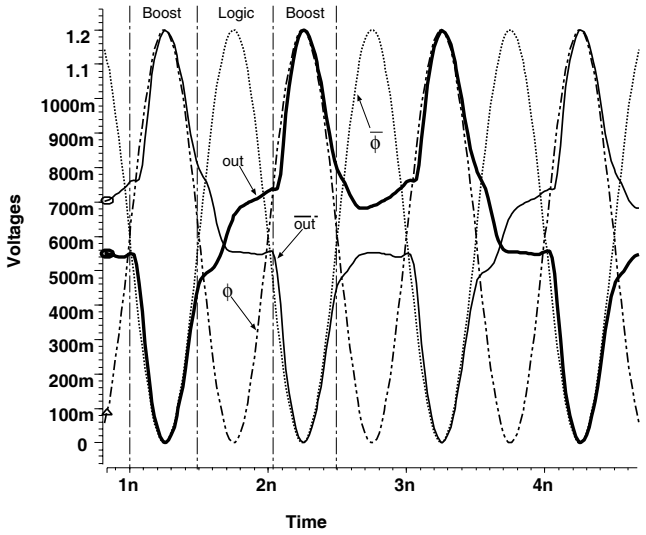


Figure 21.5.2: Simulation waveform of Boost-Logic inverter.

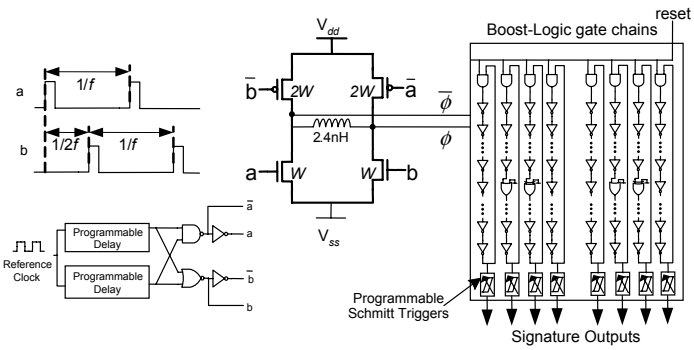


Figure 21.5.3: Boost-Logic test chip.

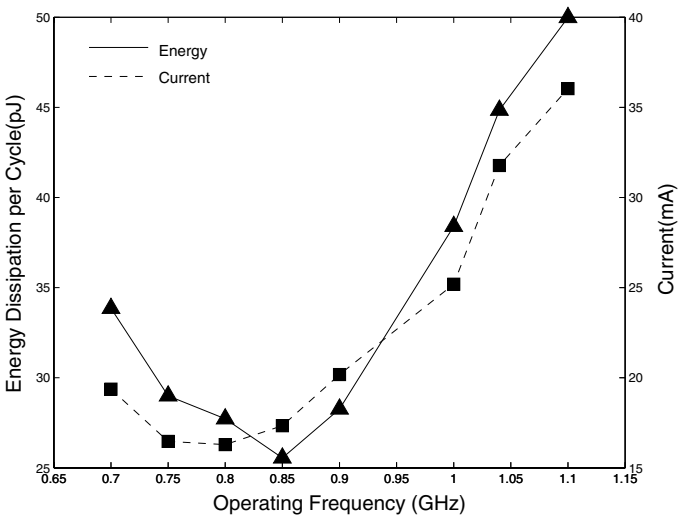


Figure 21.5.4: Measured current and corresponding energy versus frequency.

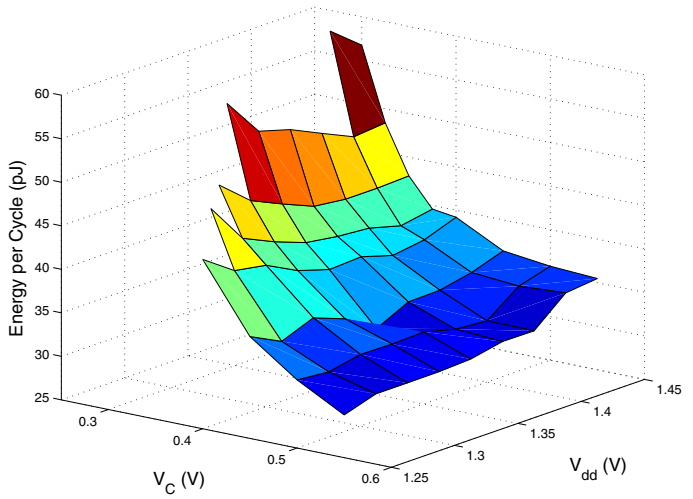


Figure 21.5.5: Measured energy dissipation as a function of V_c and V_{dd}.

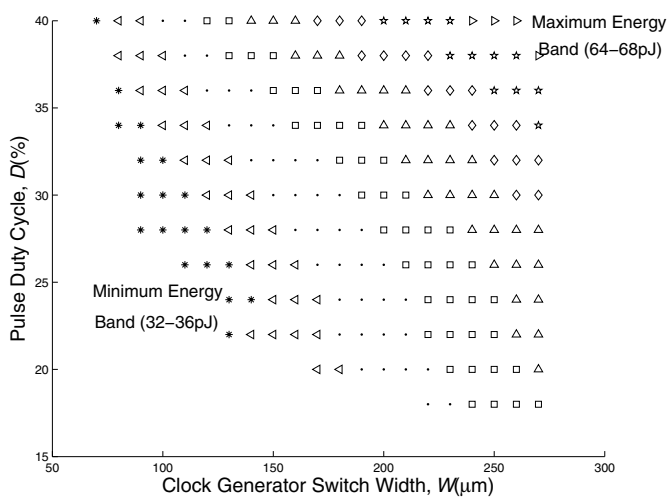


Figure 21.5.6: Shmoo plot of Boost chip.

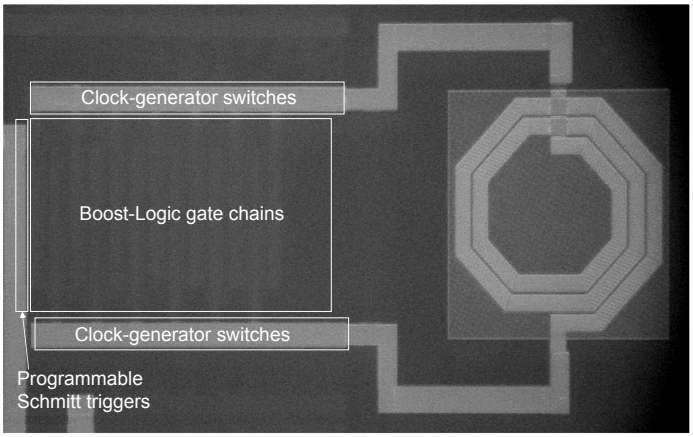
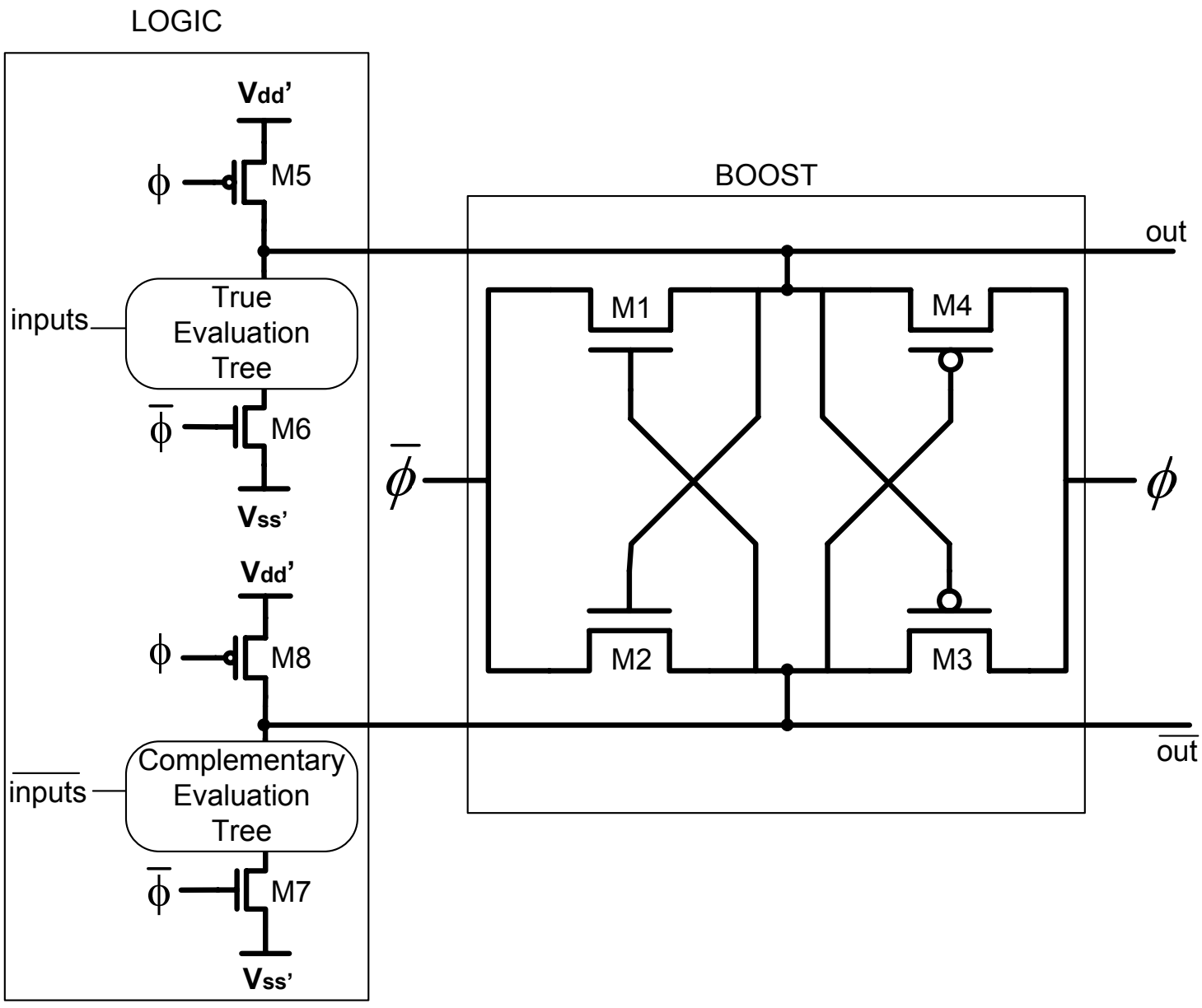


Figure 21.5.7: Die micrograph of Boost-Logic test chip.



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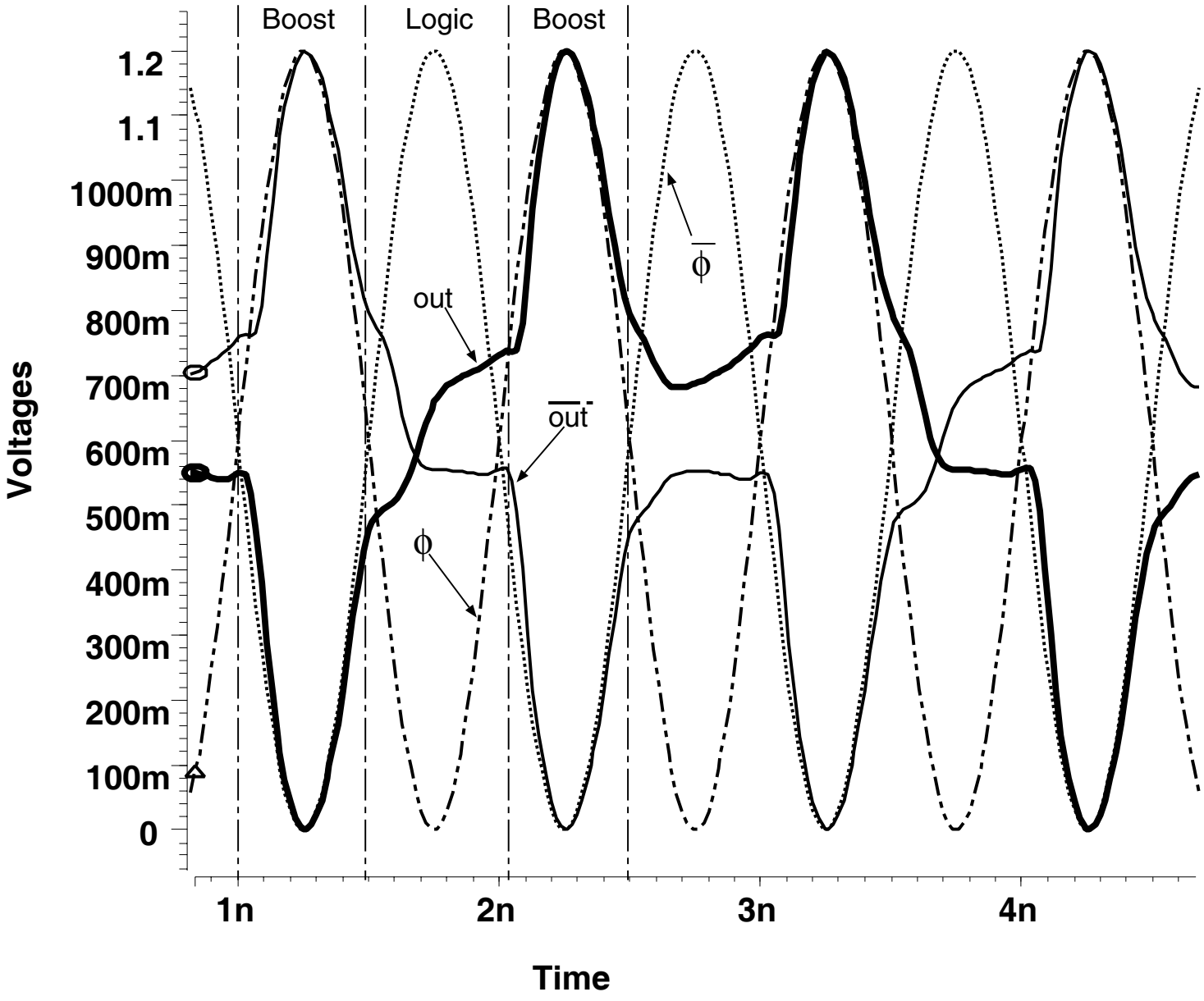

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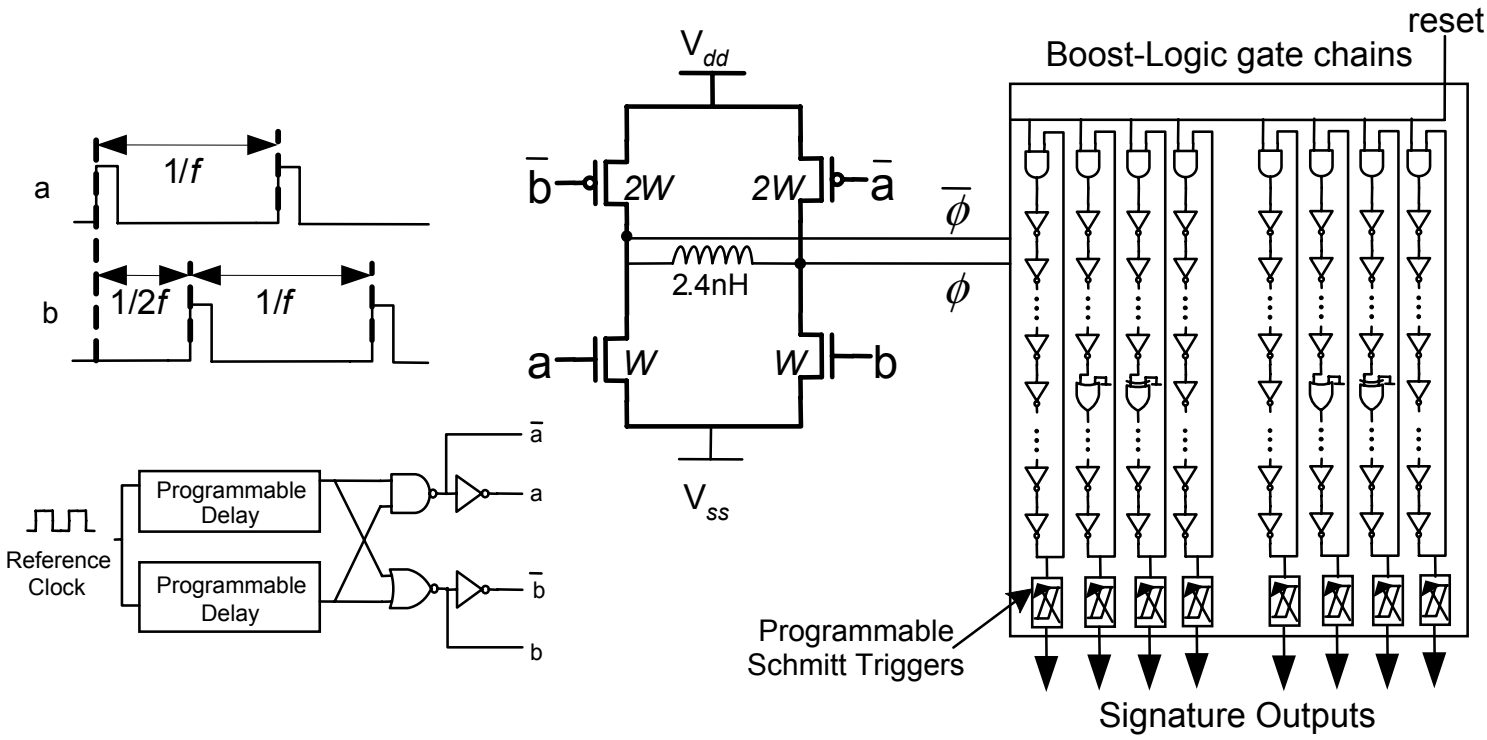

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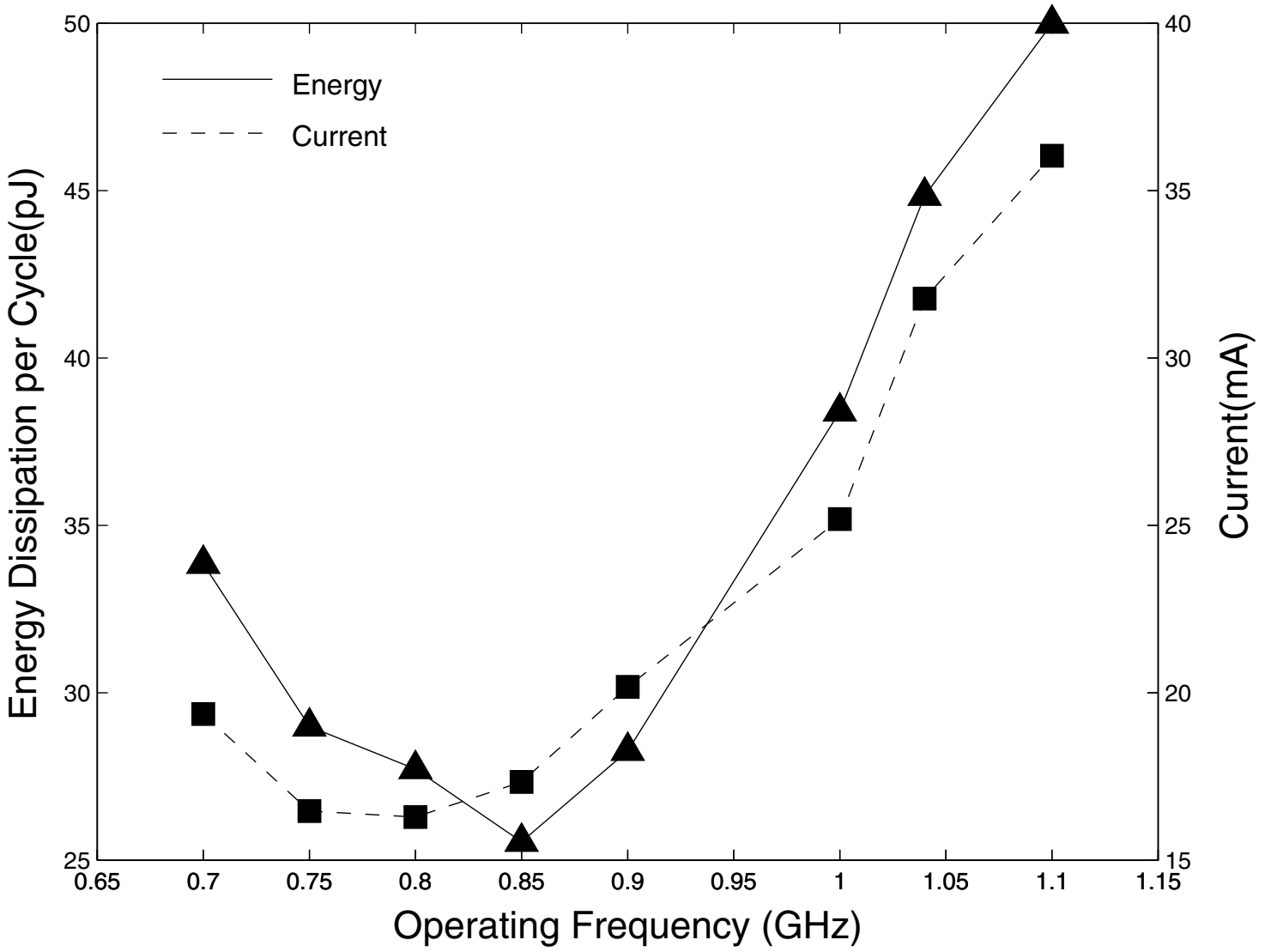

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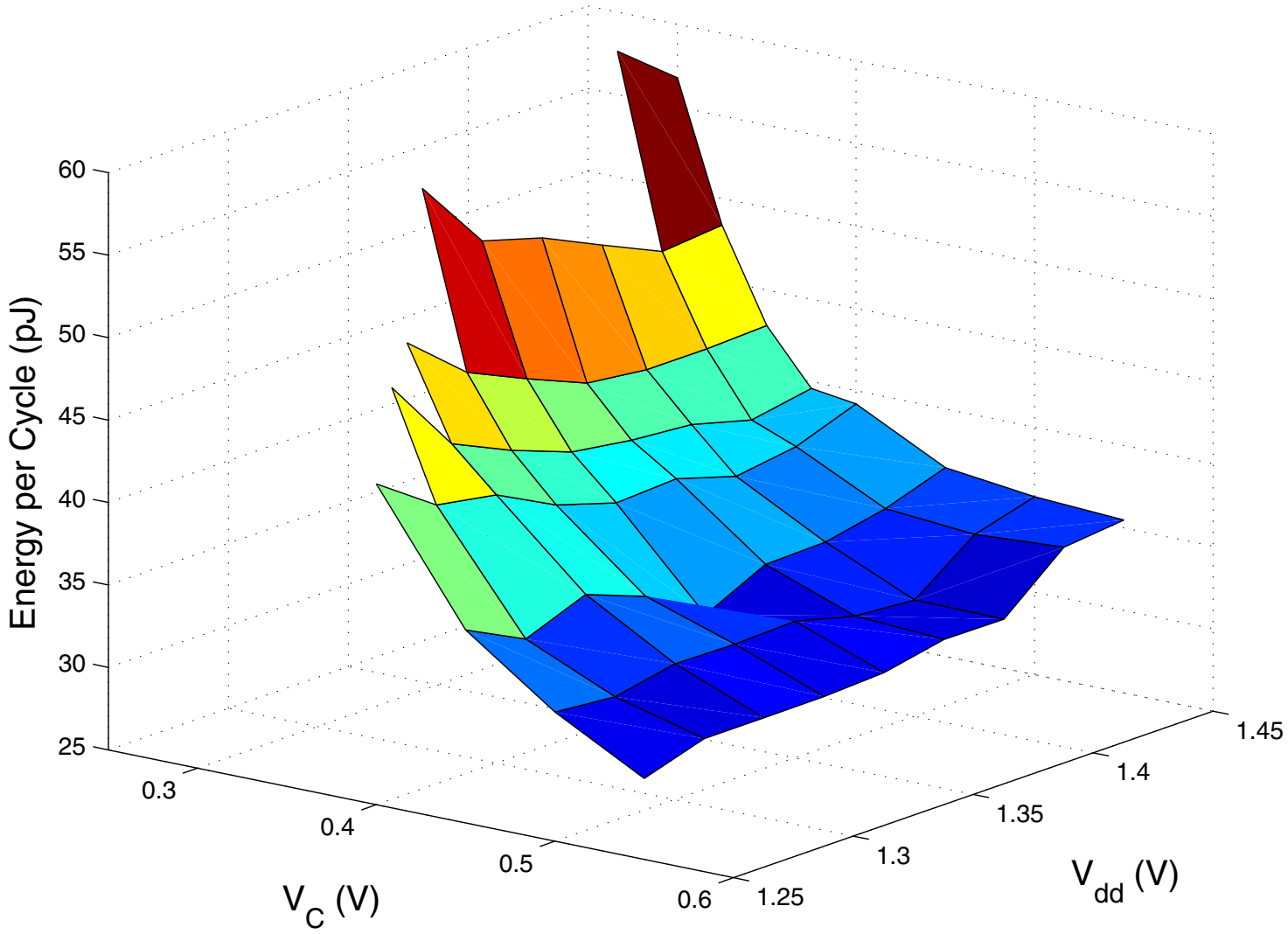

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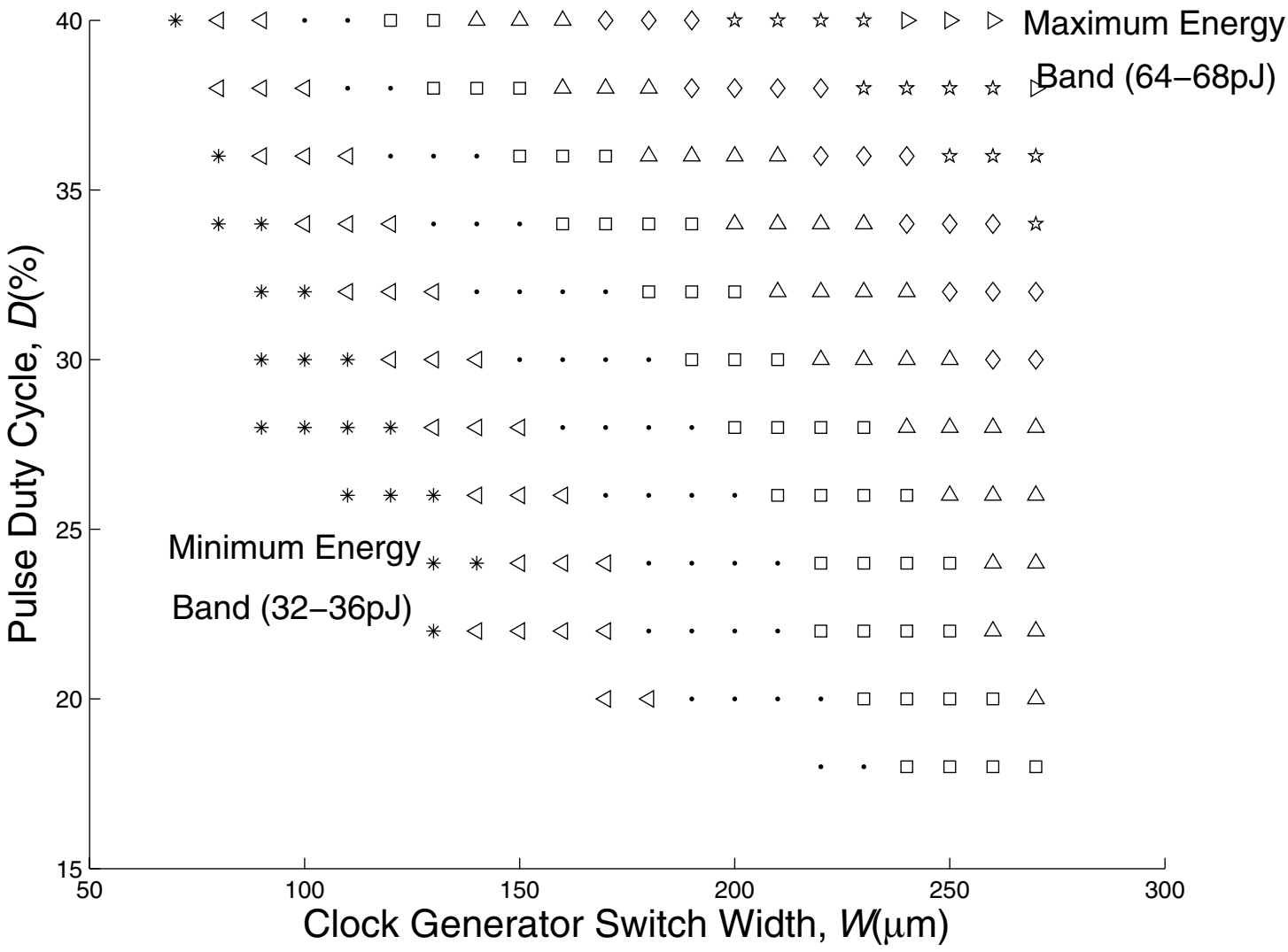

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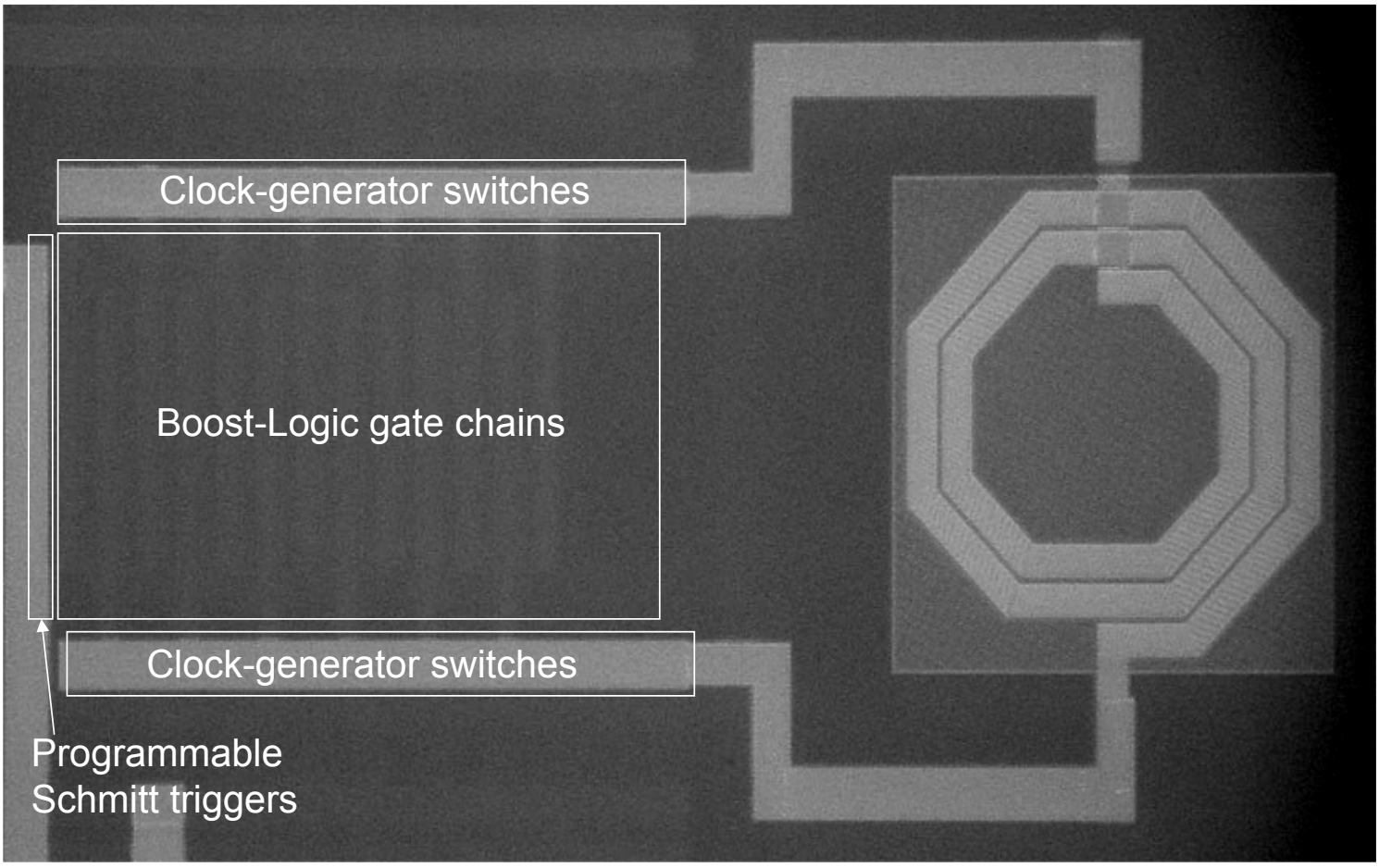

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